800 MHz Clock Distribution IC,1.5 GHz Inputs, Dividers, Delay Adjust, Five Outputs

Preliminary Technical Data

AD9512

FEATURES

Two 1.5 GHz, differential clock inputs
5 programmable dividers, 1 to 32, all integers
Phase select for output-to-output coarse delay adjust
3 independent 800 MHz LVPECL outputs
Additive output jitter 225 fs rms
2 independent 800 MHz/250 MHz LVDS/CMOS clock outputs
Additive output jitter 275 fs rms
Fine delay adjust on 1 output, 6-bit delay word
4-wire or 3-wire serial control port
Space-saving, 48-lead LFCSP

APPLICATIONS

Low jitter, low phase noise clock distribution
Clocking high speed ADCs, DACs, DDS, DDC, DUC, MxFEs
High performance wireless transceivers
High performance instrumentation
Broadband infrastructure

GENERAL DESCRIPTION

The AD9512 provides a multi-output clock distribution in a design that emphasizes low jitter and phase noise in order to maximize data converter performance. Other applications with demanding phase noise and jitter requirements also benefit from this part.

There are five independent clock outputs. Three outputs are LVPECL, and two are selectable as either LVDS or CMOS levels. The LVPECL and LVDS outputs operate to 800 MHz, and the CMOS outputs operate to 250 MHz.

Each output has a programmable divider, which may be bypassed or set to divide by any integer up to 32. The phase of one clock output relative to another clock output may be varied by means of a divider phase select function that serves as a coarse timing adjustment.

One of the LVDS/CMOS outputs also features a programmable delay element with a range of up to 10 ns of delay. This fine tuning delay block has 6-bit resolution, giving 64 possible delays from which to choose.

FUNCTIONAL BLOCK DIAGRAM

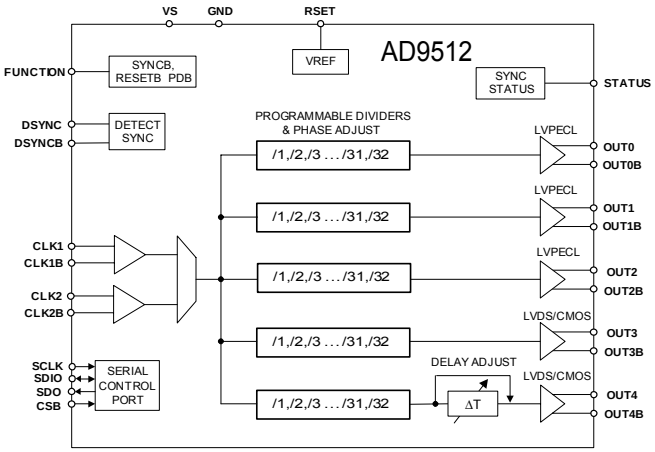

Figure 1.

The AD9512 is ideally suited for data converter clocking applications where maximum converter performance is achieved by encode signals with subpicosecond jitter.

The AD9512 is available in a 48-lead LFCSP and may be operated from a single 3.3 V supply. The temperature range is −40°C to +85°C.

Rev. PrA

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PIN CONFIGURATION

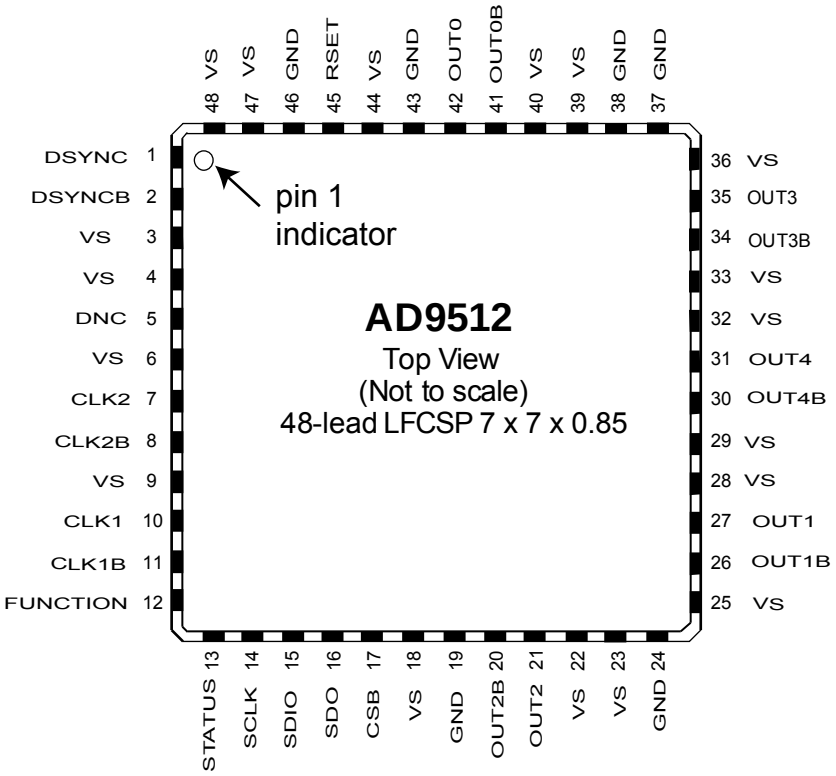

Figure 2.

Note that the exposed paddle on this package is an electrical connection as well as a thermal enhancement. For the device to function properly, the paddle must be attached to ground, GND.